REMARKS

Claims 1-25, all the claims pending in the application, stand rejected. Claims 1, 4 and 23 are amended.

Entry of Amendment

The present amendment to claims 1, 4 and 23 should be entered because they do not raise new issues and place the claims in better condition for allowance or appeal.

Claim 1

With regard to claim 1, Applicants understand from the Examiner's comments at the paragraph bridging pages 13 and 14 of the Office Action that the Examiner would withdraw the existing rejection, if step (i) of the independent claims is modified so as to deal with the Examiner's view that the existing wording covers first (i) depositing a layer of solution containing material for forming the semiconductive layer on the first electrode, followed by (ii) depositing material for forming the dielectric layer.

Applicants have amended claim 1, on the basis of paragraph 55 of the specification as published by the USPTO, to clarify the language and make clear that there is a single solution. Thus, no new issues are created.

Claim 4

This claim simply has been placed into independent form. As demonstrated subsequently, the features of claim 4, as originally presented, are not found in the prior art. Thus, no new issues are created.

Claim 23

While Applicants could amend claim 23 by adding the limitations of claim 4, this could raise new issues. Thus, Applicants are simply making this independent claim dependent on independent claim 4. Thus, no new issues are created.

Finally, Applicants respectfully note that the latter part of the existing independent claims already also indicate that the solution ***includes both materials*** because it refers to the weight ratio of the two materials **in the solution**.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 2, 4-12, 15-17, 20, 21 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirai (US 7,037,767 B2). This rejection is traversed for at least the following reasons.

Claim 1

In responding to the Applicants arguments against anticipation of claim 1 by Hirai, the Examiner identifies two points of argument at pages 12 and 13 and states with respect to the first argument that "

> In response to argument (A), Examiner maintains the rejection of the claims using the reference of Hirai. The limitation of "wherein, in step (i)...dielectric layer" is a mental process that does not further the claim limitation because the claim does not include a method or process for selecting the solvent drying time, the temperature for the first electrode, and the weight ratio for the layers so that this material does this self-organization to form the interface. Therefore, since Hirai teaches the formation of a semiconductor layer and a dielectric layer, it would inherent that these materials would be chosen based upon certain characteristics, so that they would form two functioning layer of a transistor device.framing the rejection of claim 1.

No Teaching of Phase Separation

The Examiner's foregoing comment at page 13 of the Office Action does not address the point that the claims expressly require **phase separation** of the two materials. This point was made in the previous Amendment at pages 8 and 9. There simply is no mention of phase separation to form an interface in Hirai. Such feature cannot be inherent under applicable law. Such feature also is not a "mental process," as it specifies the formation of the interface material.

No Single Deposition Step

As previously noted, Hirai teaches a "self-organization, orientation layer between the gate insulating layer and the semiconductor channel," which indicates that the gate insulating layers and semiconducting channel **are formed in *separate* deposition steps**. There is no teaching or suggestion that any portion of Hirai teaches the formation of two layers as a result of

a single deposition step. There is a completely different process in Hirai.

In the Response to Arguments, the Examiner states that "it is noted that the features upon which applicant relies (i.e., "single deposition step" and "two materials are in the same solution") are not recited in the rejected claim(s)."

However, Applicants respectfully submit that step (i) requires "depositing on the first electrode **a layer** of **a solution**...[containing two materials]" This language clearly recites a single deposition step, as the materials for forming the semiconductive layer and the dielectric layer are in "a" layer of "a" solution.

In Hirai, the conductive layer (***not*** the semiconductive layer) and the insulator layer are deposited ***separately***, and then the metal (of the conductive layer) diffuses through the insulator layer. This is in direct contrast to the invention defined by the claims of the present application, whihc specify the deposition of a solution comprising the semiconductive layer material and the dielectric layer material, so as to form the semiconductor layer and dielectric layer in a single step.

As this is not taught or suggested in Hirai, there can be no anticipation. Moreover, modification of Hirai to achieve this feature would not be obvious as it is contrary to the main teachings of the reference.

Examiner Suggestions Invited

If the Examiner has alternative language to suggest that would lead to allowance, he is invited to provide such language to the Applicants so that unnecessary expenditures of time and cost for resource strapped inventors can be avoided.

Claims 2, 3, 7-12. 15-17 and 20-22

These claims depend from claim 1 and would be allowable because of that dependence.

Claim 4

Regarding claim 4, the Examiner states that "Hirai teaches the material for forming the dielectric layer is mixed with the material for forming the semiconductive layer in the solution. (Note: Column 3, lines 65- Column 4, line 2)."

No Relevant Teaching

In relation to the rejection of claim 4, Applicants could not find any disclosure in column 3, lines 65 to column 4, line 2 of Hirai of using a solution having the material for forming the dielectric layer mixed with the material for forming the semiconductive layer. The text cited by the Examiner details that a fluid electrode material is allowed to permeate an ***already present insulation layer*** to produce a gate electrode.

Clearly, the claimed feature of the invention is not taught and the now independent claim 4 should be allowed.

Limitations of Claim 1

Moreover, independent claim 4 now contains all of the limitations of claim 1 and would be allowable for reasons given for claim 1.

Claims 5 and 6

These claims depend from claim 4 and would be allowable because of that dependence.

Claim 23

This claim now depends from claim 4 and would be allowable because of that dependence.

Claims 24 and 25

These claims depend from claim 4 and would be allowable because of that dependence.

Claim Rejections - 35 USC § 103

Claims 3, 13, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 7037767 B2). This rejection is traversed for at least the following reasons.

These claims depend from claim 1 and would be allowable because of that dependence. The features of claim 1 would not be obvious for reasons already given.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai (US 7037767 B2) in view of Veres (US 7029945 B2). This rejection is traversed for at least the following reasons.

This claim depends from claim 1 and would be allowable because of that dependence. The Examiner admits that Hirai does not explicitly disclose wherein the transistor is in top-gate configuration. The Examiner looks to Veres for such teaching. However, Veres does not remedy the deficiencies of Hirai with respect to claim 1 and the claim and its dependent claims would be patentable for reasons already given.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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